"Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines Having a DC Holding Circuit with Programmable Current Limits" (now U.S. Patent No. 6,498,825) which is a continuation-in-part application of U. S. Serial Nos. 08/841,409 (now U.S. Patent No. 6,137,827), 08/837,702 (now U.S. Patent No. 5,870,046) and 08/837,714 (now U.S. Patent No. 6,430,229) all filed on April 22, 1997, and the following U. S. patent applications filed on March 4, 1998: Serial No. 09/034,687 [[________]], entitled "Digital Isolation System With Data Scrambling" by ~~George Tyson Tuttle~~ Andrew W. Krone et al (now U.S. Patent No. 6,359,983); Serial No. 09/034,456 [[________]], entitled "Digital Isolation With ADC Offset Calibration; by Andrew W. Krone et al. (now U.S. Patent No. 6,144,326); Serial No. 09/034,455 [[________]], entitled "Ring-Detect Interface Circuitry and Method for a Communication System" by Timothy J. Dupuis et al. (now U.S. Patent No. 6,480,602); Serial No. 09/035,779 [[________]], entitled "Call Progress Monitor Circuitry and Method for a Communication System" by Timothy J. Dupuis et al. (now U.S. Patent No. 6,389,134); Serial No. 09/034,683 [[________]], entitled "External Resistor and Method to Minimize Power Dissipation in DC Holding Circuitry for a Communication System" by Jeffrey W. Scott et al. (now U.S. Patent No. 6,167,134); Serial No. 09/034,620 [[________]], entitled "Caller ID Circuit Powered Through Hookswitch Devices" by Jeffrey W. Scott et al. (now U.S. Patent No. 6,160,885); and Serial No. 09/034,682 [[________]], entitled "Framed Delta Sigma Data With Unlikely Delta Sigma Data Patterns" by Andrew W. Krone et al. (now U.S. Patent No. 6,408,034); and Serial No. 09/035,175 [[________]], entitled "Direct Digital Access Arrangement Circuitry and Method For Connecting To Phone Lines" by Jeffrey W. Scott, Navdeep S. Sooch and David R. Welland (now U.S. Patent No. 6,385,235), all of which are expressly incorporated herein by reference.

On page 5, lines 17-26:

In another embodiment a method of forming a DC holding circuit is provided. The method may include providing integrated circuitry and non-integrated circuitry to comprise the DC holding circuit, the DC holding circuit capable of meeting at least at

least a first and second phone line interface standards, the at least two phone line interface standards having differing current limit specifications, the second standard limiting DC current to a lower amount than the first standard. The method may further comprise utilizing at least one switchable circuit so that the DC holding circuit may be programmed for at least one of the phone line interface standards, and coupling the integrated circuitry and the non-integrated circuitry together so that when the DC holding circuit is programmed for the second phone line interface standard, at least one circuit element of the external circuitry will receive additional DC current as compared to when the DC holding circuit is programmed for the first phone line interface standard.

On page 6, lines 4-9:

Another ~~a method~~ embodiment provides a DC holding circuit. The method includes forming the DC holding circuit with internal circuitry internal to an integrated circuit and external circuitry external to the integrated circuit, the DC holding circuit compatible with at least one phone line interface standard having a DC current limit requirement. The method may further include coupling the internal circuitry and external circuitry so that more power may be dissipated in the external circuitry than in the internal circuitry.

On page 9, lines 10-25:

The hybrid and DC termination circuitry 1617 may have a number of external pins that also connect to external telephone interface circuitry such as hook-switch circuitry and a diode bridge <u>as shown in Figures 2 and 4</u>. For example, the hybrid and DC termination circuitry 1617 may have a DC termination pin (DCT), a voltage regulator pin (VREG), two external resistor pins (REXT and REXT2), two filter pins (FILT and FILT2) and a isolated ground pin (IGND). The DC termination circuitry terminates the DC voltage on the phone line and provides an internal power supply for the phone line side circuitry 118. The DC termination pin (DCT) receives a portion of the phone line DC current with the remainder flowing through pins QE2 and QB2, depending upon the

termination mode and DC current level. The voltage regulator pin (VREG) allows external regulator circuitry, such as a capacitor, to be connected to the DC termination circuitry ~~1618~~ 1617. External resistors and a capacitor may be connected to the two external resistor pins (REXT and REXT2) to set the real and complex AC termination impedance respectively. The filter pin FILT (along with the capacitor C5) sets the time constant for the DC termination circuit. The filter pin FILT2 sets the off hook/on hook transient responses for pulse dialing. The isolated ground pin (IGND) may be connected to the system ground for the powered side circuitry 116 through a capacitor within the isolation barrier 120 and may also be connected to the phone line through a ground connection within external diode bridge circuitry.

On page 10, lines 10-23:

In the embodiment of Figure 3, communications from the phone line side circuitry 118 to the powered circuitry 116 are considered receive signals. Within phone line side circuitry 118, a delta-sigma analog-to-digital converter (ADC) 1710 receives an internal analog receive signal (RX_{INT}), which may be provided for example by hybrid circuitry ~~1616~~ 1617. The output of delta-sigma ADC 1710 is oversampled digital data stream in a pulse density modulation format. The decoder/encoder circuitry 1708 processes and formats this digital information as desired before sending it across the isolation barrier 120 as encoded digital information. For example, decoder/encoder 1708 may multiplex control data with the digital stream before it is sent across the isolation barrier 120. This control data may be ~~a~~ any desired information, such as ring detect signals, off-hook detect signals, other phone line status information or data indicative ~~or~~ of the country in which the DAA will be utilized (so that the appropriate phone line interface standards will be satisfied). Within powered side circuitry 116, the decoder/encoder 1706 decodes this encoded digital information received across the isolation barrier 120. The digital filter 1702 processes this decoded digital stream and converts it into internal digital receive data (RX_D) that may be provided through the digital interface 1606 to an external controller.

Page 10, line 24 through page 11, line 9:

Communications from the powered side circuitry 116 to the phone line side circuitry 118 are considered transmit signals. Within powered side circuitry 116, a delta-sigma modulator 1704 receives an internal digital transmit signal (TX_D), which may be provided for example from an external controller through digital interface 1606. The output of delta-sigma modulator 1704 is an oversampled digital data stream in a pulse density modulation format. The decoder/encoder circuitry 1706 processes and formats this digital information as desired before sending it across the isolation barrier 120 as encoded digital information. For example, decoder/encoder 1706 may multiplex control data with the digital stream. This control data may be ~~a~~ any desired information, such as ring detect signals, off-hook detect signals, or other phone line status information. In addition, decoder/encoder 1706 may add framing information for synchronization purposes to the digital stream before it is sent across the isolation barrier 120. Still further, decoder/encoder 1706 may format the digital data stream so that a clock signal may be recovered within the phone line side circuitry 118~~, for example, as is discussed with respect to Figure 14 above~~. Within phone line side circuitry 118, the decoder/encoder 1708 may recover a clock signal and may decode the encoded digital information received across the isolation barrier 120 to obtain framing, control or status information. The digital-to-analog converter (DAC) 1712 converts the decoded digital stream and converts it into internal analog transmit data (TX_{INT}) that may be provided as an analog signal through the hybrid circuitry ~~1616~~ <u>1617</u> and ultimately to the phone lines.

On page 14, lines 5-15:

In order to ~~programmable~~ <u>programmably</u> achieve the DC termination characteristics of Figures 5A-5C, the DC termination or DC holding circuit of the present invention provides a variety of improvements over the prior art. For example in order to achieve the current limiting requirements (such as in the TBR21 standard), the phone line side circuitry 118 must dissipate up to approximately two watts of power. Typical non current limiting specifications such as FCC standards will result in only a fraction of that

amount of power dissipation to occur. However, it is undesirable to require this increase power dissipation to be performed by the phone line side integrated circuit 1802B. The circuit of Figure 6 provides a mechanism in which the increased power dissipation requirements of current limiting standards may be achieved by dissipating the additional power external to the integrated circuit. In this manner, a single DAA system may be utilized for both current limiting DC termination standards and non-current limiting standards without requiring excessive power dissipation within an integrated circuit.--

On page 14, lines 16-30:

As shown in Figure 6, a phone line side integrated circuit 1802B includes DC termination or DC holding circuitry 600 which is coupled to the DCT, QE2 and QB2 pins. The DCT pin is coupled to a resistor RA, for example a 1600Ω resistor. The QB2 pin is coupled to a resistor RB, for example a 1600Ω resistor. Though shown as single resistors, each resistor RA and RB may be formed from a plurality of resistors such as resistors R1, R11, and R17, and R4, R19, and ~~R19~~ R20 respectively as shown in Figure [[4]] 6. Resistors RA and RB are coupled to the hookswitch circuitry such as shown in Figure 4. The QE2 and QB2 pins are coupled to the emitter and base of transistor Q4 respectively. In operation, the DC current on from the phone line may be directed through resistors RA and RB in varying amounts through control of transistor Q4 in order to adjust the DC impedance seen by the phone lines. For example, the 50Ω impedance section of the I-V curve of Figure 5D (segment A) may be obtained when the transistor Q4 is fully on and the bulk of the DC current passes through transistor Q4. The 3200Ω impedance section of the I-V curve of Figure 5D (segment B) may be obtained while the transistor Q4 is being turned off and thus actively steering current through resistors RA and RB. The 800Ω impedance section of the I-V curve of Figure 5D (segment D) may be obtained when the transistor Q4 is fully turned off and thus the DC current is split between the resistors RA and RB.--

On page 15, lines 15-24:

A DC holding circuit 700 for implementing the DC termination characteristics discussed above is shown in Figure 7. Figure 7 illustrates portions of the DAA system with like reference numbers and letters as shown in Figure 4. As can be seen, Figure 7 includes circuitry both internal and external to the phone side integrated circuit 1802B. More particularly, Figure 7 includes the RX, DCT, QB2, QE2, and ~~FILT2~~ FILT pins and associated internal and external circuits (the hookswitch circuitry is not being shown). As shown in Figure 7, the DC holding circuit 700 includes switches S1, S2, S3, S4, S5, S6, and S7. As discussed in detail below, the switches may be utilized to select the current limiting or non-current limiting modes of operation, to ~~switchable~~ switchably operate the DC holding circuit in order to achieve fast settling times and low frequency operation and to select the low voltage modes of operation.

On page 19, lines 9-23:

The distortion adjustment circuit block 710 of ~~Figure 14~~ Figure 7 compensates for this clipping effect through control of transistor M14 which is also coupled to the QE2 pin. The distortion adjustment circuit block 710 operates in the mode 3 current limiting mode through the closure of switch S7. In other modes, switch S7 is opened and the distortion adjustment circuit block 710 does not affect the DC holding circuitry. The distortion adjustment circuit block 710 operates such that the current through transistor M14 has a response opposite to that of the current through transistor M3 such as shown by curve B of Figure 8. Because both transistors M3 and M14 are coupled to the QE2 pin, the total AC component effect of the current through transistors M3 and M14 will sum together. Since curves A and B Figure 8 demonstrate opposite clipping effects, the summation of these currents will be relatively free of clipping and the associated distortion, at least to a first order. The current response of curve B is obtained through the current steering relationship of transistors M3, M12, M11 and M14. Thus, with the transistor sizing shown in Figure 7, the relationship i(M14) = (10 x I2) – i(M3) will result and the resulting AC component seen by the phone line due to the AC component of the current in transistors M3 and M4 will be 10 x I2. The value of I2 may be chosen such that I2 is greater than I(M3)/10 at the crossover point.